material finger of each elementary cell having at least one second prolongation and said at least one fourth metal stripe having at least one first prolongation adapted for being placed on said at least one second prolongation of said at least one material conductor finger to form at least another contact point.

Always according to present invention it is possible to provide a process for manufacturing of an integrated device of the MOS type~~, as defined in claim 21~~.

Thanks to present invention it is possible to form a semiconductor integrated device of the MOS type which, even if it has only one metallization level, allows to form more contact points for the gate fingers. Also said integrated device has a structure that minimizes the electromagnetic iterations among the blocks of elementary cells of which it is composed.

BRIEF DESCRIPTION OF THE DRAWINGS

The features and the advantages of the present invention will be made evident by the following detailed description of embodiments thereof, shown as not limiting examples in the annexed drawings, wherein:

FIG. 1 is a schematic view of a part of a layout of a LDMOS device according to prior art;

FIG. 2 is a more detailed view of a zone of the layout in FIG. 1;

FIG. 3 shows a section of the device in FIG. 2 according to line III-III;

FIG. 4 is a schematic view of a part of a layout of a LDMOS device according to a first embodiment of the present invention;

FIG. 5 shows a section of the device in FIG. 4 according to line V-V;

FIG. 6 is a schematic view of a part of a layout of a LDMOS device according to a second embodiment of the present invention; and

FIG. 7 is a schematic view of a part of the layout of the device according to invention.

DETAILED DESCRIPTION

In FIG. 1 a schematic view of a part of a layout of a LDMOS device according to prior art is shown. The blocks 100 constituting the active zones of the LDMOS